REMARKS

Claims 1-35 are pending in the application. Claims 1-3, 15, 16 and 18-22 stand rejected. Applicant appreciates that claims 4-14 and 17 are indicated as containing allowable subject matter and that claims 23-35 are allowed. By way of the present amendment, new claims 36-39 are being added.

Claims 1-3, 15 and 16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Chen (U.S. Pat. No. 5,754, 080). Claims 19-22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chen in view of Wu (U.S. Pat. No. 5,486,794). The rejection of those claims is respectfully traversed for the reasons given below.

Claim 1 of the present application recites a method of acquiring timing associated with an input data stream, comprising detecting whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream; and evaluating whether a phase-locked loop (PLL) has acquired the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period. The specification describes on page 18, line 16 – page 21, line 24 an exemplary high level flow diagram of acquiring a frequency according to an embodiment of the invention. As shown in Fig. 16, the bit errors, which are those transitions that occur in the forbidden zone (the predetermined portion of the sample clock period of the sample clock utilized to sample the input data stream), are detected and lock is determined according to how many bit errors (or transitions in the predetermined portion of a sample clock period) occur. If sufficiently few error have occurred, then the PLL has locked to the input data stream and thus acquired the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period.

In contrast, in one prior art approach, the specification explains that in order to help the VCO acquire the timing of the input data stream, a reference clock (not the reference clock taught by Chen since that clock is derived from the data) is used to center the nominal VCO output and determination of whether lock is achieved and thus the timing has been acquired, is done by comparing the reference clock to a divided down version of the recovered clock and determining if the error is sufficiently small. See page 2, lines 22 – page 3, line 10.

Chen teaches a circuit for detecting whether a reference clock signal (extracted from the received data) is aligned with incoming data. Col. 2, lines 32-35. However, the aligning taught by Chen is different from evaluating whether a phase-locked loop (PLL) has acquired the timing of the input data stream according to occurrence of transitions of the input data stream in the predetermined portion of the sample clock period as claimed. Instead, Chen simply teaches detecting whether the a clock (clock 4 in the example given) lags or leads the data (see Figs. 6 and 7). Chen teaches adjusting the output of clock generator 22 based on the UP or DOWN signals 35A and 35B (Fig. 5), which indicate whether the clock 4 lags or leads transitions of the input data stream. The circuit of Chen is used to align the clock and data in a conventional manner after the PLL has locked to the incoming data. There is no teaching as to how the PLL acquires the timing of the incoming data so that the aligning can be done. Further, Chen fails to teach anything regarding how a determination has been made of whether lock has been achieved.

Accordingly, applicant respectfully maintains that claim 1 and all claims dependent thereon distinguish over Chen, alone or in combination with other references of record.

With regards to claim 2, although the Office Action maintains that Chen teaches that evaluating whether the PLL has acquired the timing of the input data stream further comprises determining over a plurality of time periods, each of the time periods including an increasing number of evaluation intervals, whether the PLL is locked to the timing of the input data stream according to a number of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period. As explained with relation to Fig. 16 of the application, the exemplary embodiment illustrated therein utilizes an increasing number of evaluation intervals to guard against the possibility of false lock. (See page 19, lines 29 – page 30, line 2). Thus, in the exemplary embodiment illustrated in Fig. 16, state 2 evaluates over 16 cycles, state 3 over 48 cycles and state 4 over 512 cycles. Chen teaches nothing about evaluation intervals or time periods having an increasing number of evaluation intervals. Nor does Chen teach anything regarding a number of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period. Chen does not track the number of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period. Chen simply determines if the clock lags or leads the data and gives a fixed adjustment to the

VCO based on that determination. Accordingly, applicant respectfully submits that claim 2 distinguishes over Chen for this additional reason.

With regards to the rejection of claim 16, applicant notes that claim 16 is in means plus function format. Accordingly, claim 16 should be interpreted to cover the corresponding structure, materials or acts in the specification and equivalents thereof. See MPEP 2181. Structure corresponding the claimed means includes, but is not limited to, Figs. 12A, 12B, 16, 18, 19 and the accompanying descriptions. Other figures and description provide additional description and structure. There is nothing in Chen that teaches such structure. Applicant further maintains that there is nothing in Chen that teaches the function of evaluating whether a phase-locked loop (PLL) has recovered a timing associated with the input data stream according to occurrence of transitions in the predetermined portion of the clock as recited in claim 16. Accordingly, applicant respectfully request that the rejection of claims 16 and all rejected claims dependent thereon be reconsidered and withdrawn.

With regards to claim 19, applicant respectfully submits neither Chen nor Wu teach a method for acquiring a clock embedded in an input data stream that comprising varying an output of a variable oscillator until transitions of the input data stream occurring in a predefined phase zone of a sample clock sampling the input data stream occur below an acceptable rate. Neither Chen nor Wu teach determining a rate of transitions that occur in a predefined phase zone of a sample clock sampling the input data stream. All Chen teaches is determining whether a clock lags or leads the transitions of the input data stream. Wu fails to make up for Chen's shortcomings. Accordingly, applicant respectfully submits that claim 19 and all claims dependent thereon distinguish over the references of record.

Claim 20 has been amended to better claim the invention.

New claims 36-39 have been added to recite the invention from a different perspective and are believed to be patentable over the art of record.

In view of the above remarks, applicant believes that all claims are in condition for allowance and early notification to that effect is respectfully requested. If there are any issues

which the Examiner believes could be resolved via a telephone interview, the Examiner is respectfully requested to contact the undersigned at the number indicated below.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231 on the date shown below.

Mark Zagorin — 4/4/03 Date

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS IN ACCORDANCE WITH 37 C.F.R. § 1.121(c)(1)(ii)

20. (Amended) The method as recited in claim 19 wherein [the acceptable] a rate of transitions is determined according to a number of evaluation intervals having one or more transitions occurring in the predefined phase zone.